



Mobile Networking

Mohammad Hossein Manshaei

manshaei@gmail.com

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FHSS, IR, and Data Modulations

MORE ON 802.11B PHY LAYER

Contents

- IEEE 802.11b with FHSS
- IEEE 802.11b with IR
- Available Modulations and their Performance
 - DBPSK
 - DQPSK
 - CCK: Complementary Code Keying
 - PBCC: Packet Binary Convolutional Code

Frame format, Regulations, ...

FHSS IN 802.11B

Why Frequency Hopping?

- Frequency Hopping enables coexistence of multiple networks (or other devices) in same area
- FCC recognizes FH as one of the techniques withstanding Fairness requirements for unlicensed operation in the ISM bands.
- 802.11 Frequency Hopping PHY uses 79 nonoverlapping frequency channels with 1 MHz channel spacing.
- FH enables operation of up to 26 colocated networks, enabling therefore high aggregate throughput.
- Frequency Hopping is resistant to multipath fading through the inherent frequency diversity mechanism

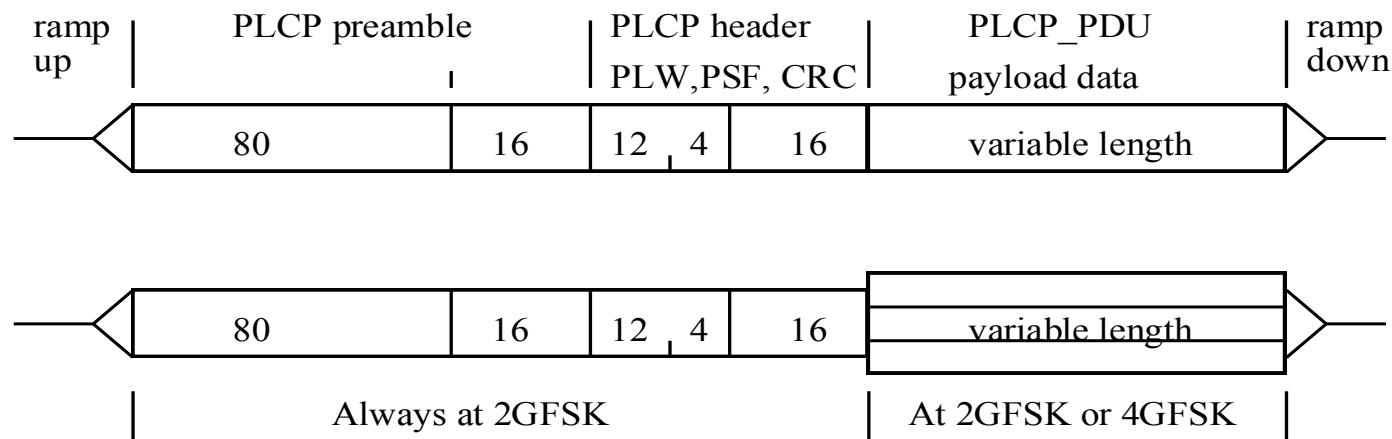
Regulatory Requirements for FH

- **North America** (CFR47, Parts 15.247, 15.205, 15.209):
 - Frequency band: 2400-2483.5 MHz
 - At most 1 MHz bandwidth
 - At least 75 hopping channels, pseudorandom hopping pattern
 - At most 1 W transmit power and 4 W EIRP (including antenna)
- **Europe** (ETS 300-328, ETS 300-339):
 - Frequency band: 2400-2483.5 MHz
 - At least 20 hopping channels
 - At most 100 mW EIRP
- **Japan** (RCR STD-33A):
 - Frequency band: 2471-2497 MHz
 - At least 10 hopping channels

802.11 FH PHY vs. Regulations

- 1 MHz Bandwidth
- 79 hopping channels in **North America and Europe**; pseudorandom hopping pattern. (2.402-2.480GHz)
- 23 hopping channels in **Japan** (2.473-2.495GHz)
- At most 1 W power; devices capable of more than 100 mW have to support at least one power level not exceeding 100 mW.

802.11 FHSS Frame Format



- PHY header indicates payload rate and length; CRC16 protected
- Data is whitened by a synchronous scrambler and formatted to limit DC offset variations
- Preamble and Header always at 1 Mbit/sec; Data at 1 or 2 Mbit/sec

PLCP Preamble

- PLCP preamble starts with **80 bits**
 - **0101** sync pattern
 - detect presence of signal
 - to resolve antenna diversity
 - to acquire symbol timing
- Follows **16 bit Start Frame Delimiter (SFD)**
 - **h0CBD**
 - the SFD provides symbol-level frame synchronization
 - the SFD pattern is balanced

PLCP Header

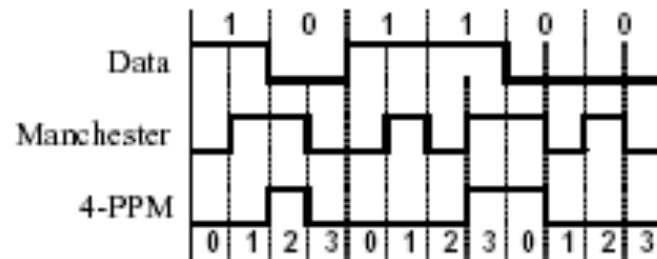
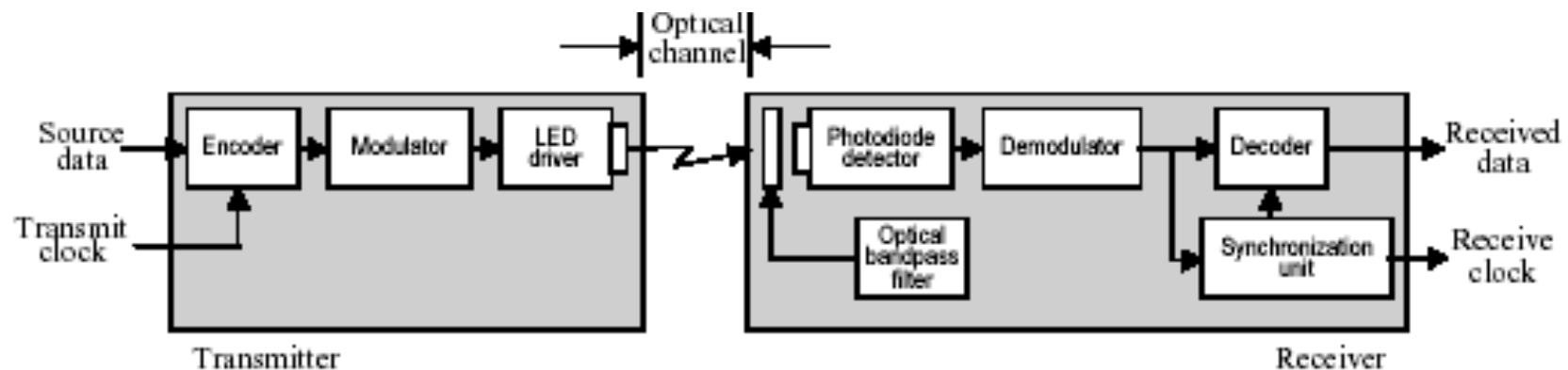
- A 32 bit PLCP header consists of
 - **PLW** (PLCP_PDU Length Word) is 12 bits field
 - indicating the length of PLCP_PDU in octets, including the 32 bit CRC at the PLCP_PDU end, in the range 0 .. 4095
 - **PSF** (PLCP Signaling Field) is 4 bit field,
 - Bit 0 is reserved
 - Bits 1-3 indicates the PLCP_PDU data rate
 - (1, 1.5, 2, 2.5, 3, 3.5, 4, 4.5 Mbit/s)
 - **HEC** is a 16 bit CRC

PLCP_PDU Formatting

- Dividing serial bit stream into symbols:
 - at 1 Mbps, each bit is converted into 2FSK (Frequency-Shift Keying) symbol
 - at 2 Mbps, each 2 bits are encoded into 4FSK symbol using Gray mapping

Baseband Infrared (IR) in 802.11b: PPM Modulation

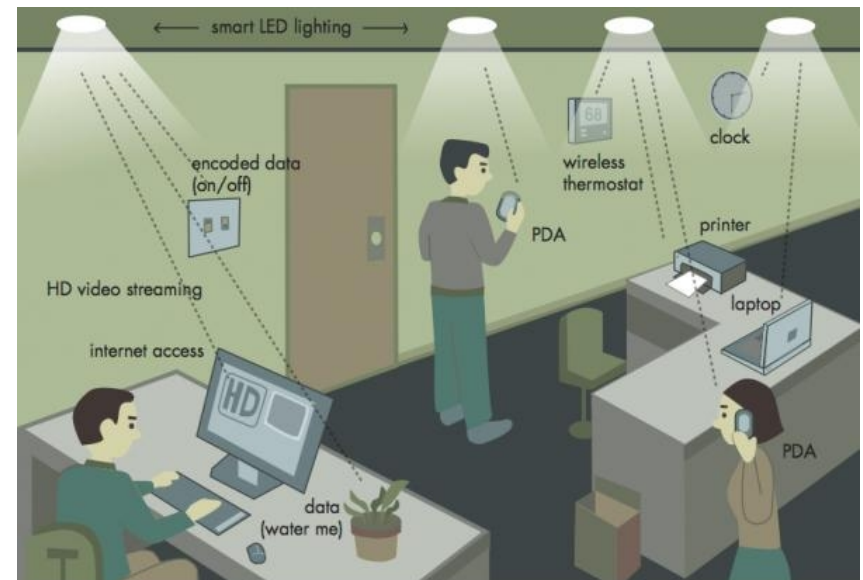
- OOKPPM :
 - Reduce the optical power



Data
00 = 0
01 = 1
10 = 2
11 = 3
Pulse position

LiFi: Visible Light Communications (IEEE 802.15.7)

- Defined by Prof. Harald Haas (University of Edinburgh in the UK)
- High speed and fully networked wireless communications, like Wi-Fi, using visible light
- (VLC) works by switching bulbs on and off within nanoseconds



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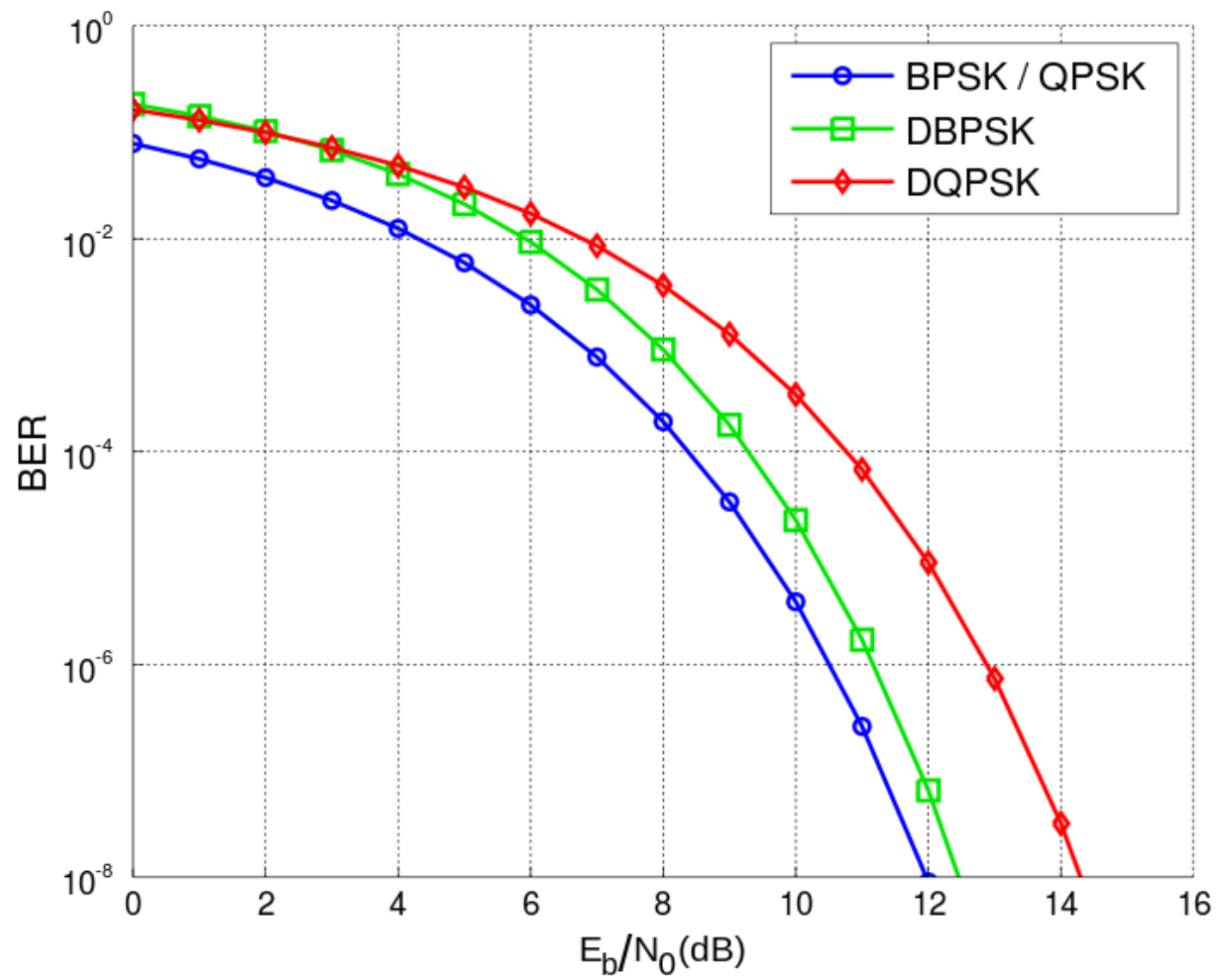
I Mbps DBPSK Modulation

Encoding Table

Bit input	Phase change ($+j\omega$)
0	0
1	π

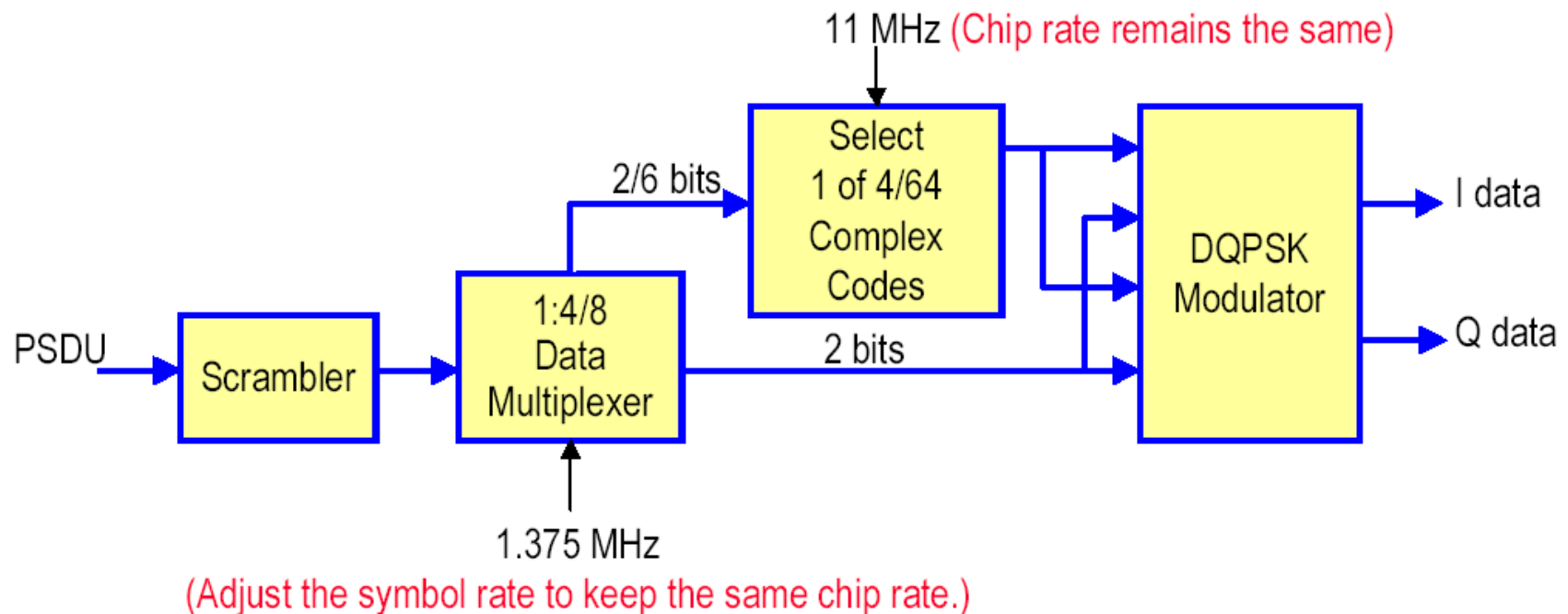
2 Mbps DQPSK Modulation Encoding Table

Dibit pattern (d0,d1) d0 is first in time	Phase change (+j ω)
00	0
01	$\pi/2$
11	π
10	$3\pi/2$ ($-\pi/2$)



Complementary Code Keying (CCK)

- HR/DSSS adopts 8-chip CCK as the modulation scheme with 11 MHz chipping rate



$$8\text{-chip} \times 1.375\text{MHz} = 11\text{MHz chipping rate}$$

Complementary Code Keying (CCK)

- Spreading code length = 8, $c=\{c0-c7\}$ and

$$c = \{e^{j(\varphi_1+\varphi_2+\varphi_3+\varphi_4)}, e^{j(\varphi_1+\varphi_3+\varphi_4)}, e^{j(\varphi_1+\varphi_2+\varphi_4)}, \\ -e^{j(\varphi_1+\varphi_4)}, e^{j(\varphi_1+\varphi_2+\varphi_3)}, e^{j(\varphi_1+\varphi_3)}, -e^{j(\varphi_1+\varphi_2)}, e^{j\varphi_1}\}$$

where φ_1 is added to all code chips,

φ_2 is added to all odd code chips,

φ_3 is added to all odd pairs of code chips, and

φ_4 is added to all odd quads of code chips.

Cover code : c4 and c7 chips are rotated 180° (with -) by a cover sequence to optimize the sequence correlation properties and minimize dc offsets in the codes.

Complementary Code Keying (CCK) 5.5Mbps

- At 5.5Mbps CCK, 4 data bits (d0,d1,d2,d3) are transmitted per symbol
 - (d0,d1) is DQPSK modulated to yield φ_1 , which the information is bear on the “phase change” between two adjacent symbols
 - $(11/8) \cdot (4 \text{ data bits per symbol}) \cdot 1\text{Mbps} = 5.5\text{Mbps}$

Dibit pattern (d0, d1) (d0 is first in time)	Even symbols phase change (+j ω)	Odd symbols phase change (+j ω)
00	0	π
01	$\pi/2$	$3\pi/2$ ($-\pi/2$)
11	π	0
10	$3\pi/2$ ($-\pi/2$)	$\pi/2$

Complementary Code Keying (CCK) 5.5Mbps

- (d2,d3) encodes the basic symbol, where

$$\begin{cases} \phi_2 = d_2 \times \pi + \pi / 2; \\ \phi_3 = 0; \\ \phi_4 = d_3 \times \pi; \end{cases}$$

d2, d3	c1	c2	c3	c4	c5	c6	c7	c8
00	1j	1	1j	-1	1j	1	-1j	1
01	-1j	-1	-1j	1	1j	1	-1j	1
10	-1j	1	-1j	-1	-1j	1	1j	1
11	1j	-1	1j	1	-1j	1	1j	1

Complementary Code Keying (CCK) 11Mbps

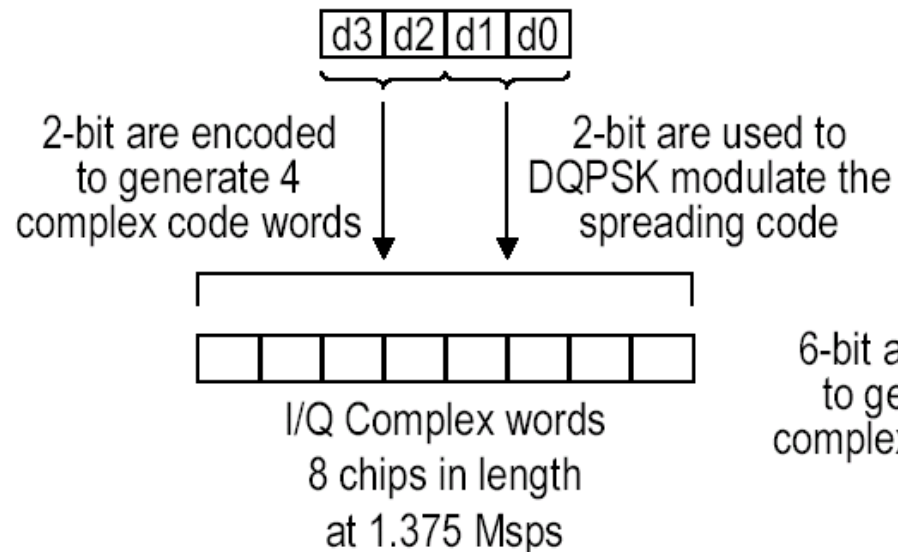
- At 11Mbps CCK, 8 data bits (d0-d7) are transmitted per symbol
 - (d0,d1) is DQPSK modulated to yield φ_1 , which the information is bear on the “phase change” between two adjacent symbols
 - (d2,d3),(d4,d5),(d6,d7) encode $\varphi_2, \varphi_3, \varphi_4$, respectively, based on QPSK
 - $(11/8) \times (8 \text{ data bits per symbol}) \times 1\text{Mbps} = 11\text{Mbps}$

Dibit pattern [d _i , d _(i+1)] (d _i is first in time)	Phase
00	0
01	$\pi/2$
10	π
11	$3\pi/2$ ($-\pi/2$)

Complementary Code Keying (CCK)

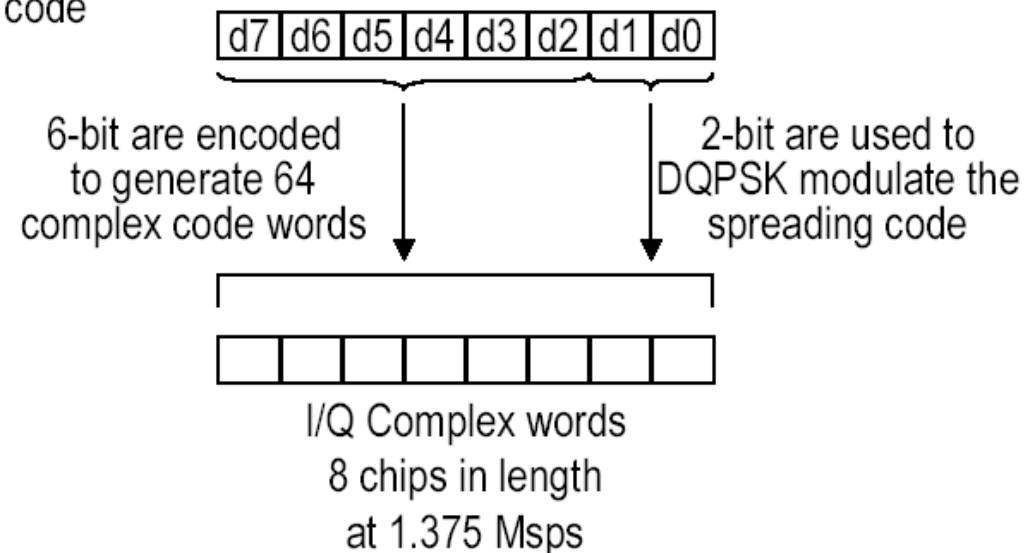
CCK at 5.5 Mbps

PSDU binary bits
grouped into "nibbles"



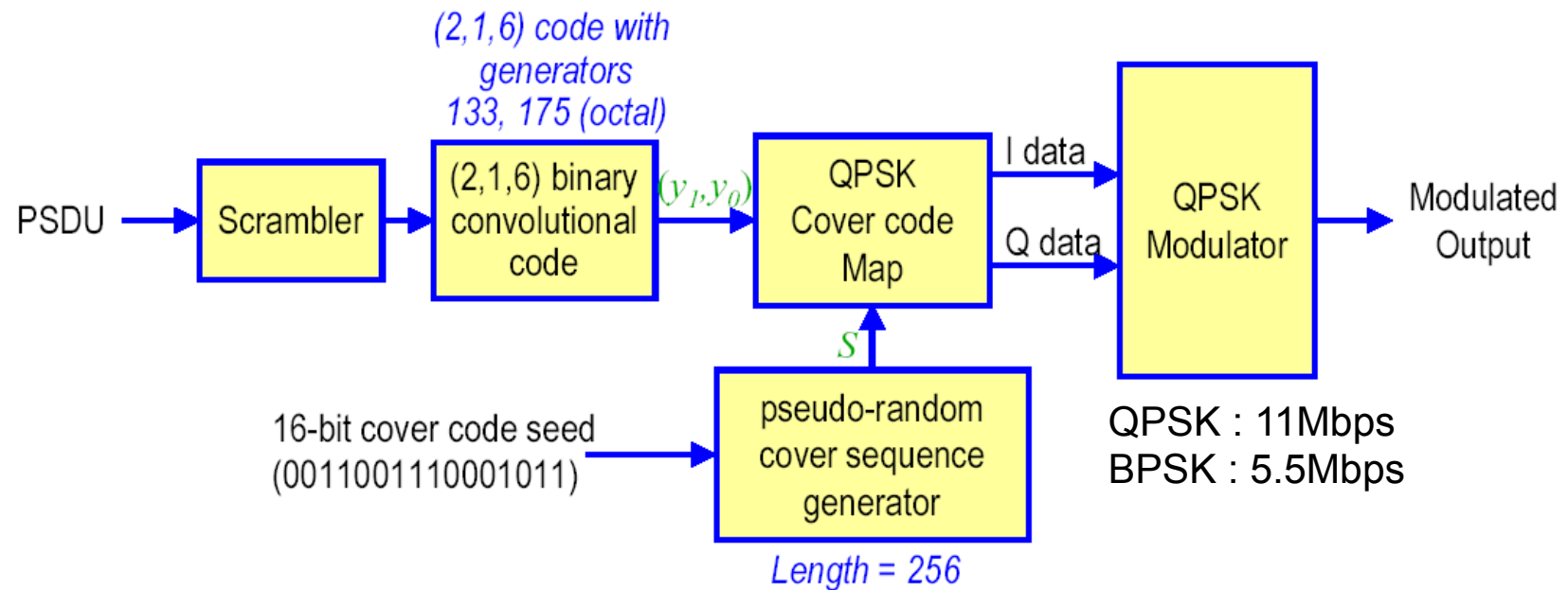
CCK at 11 Mbps

PSDU binary bits
grouped into "bytes"



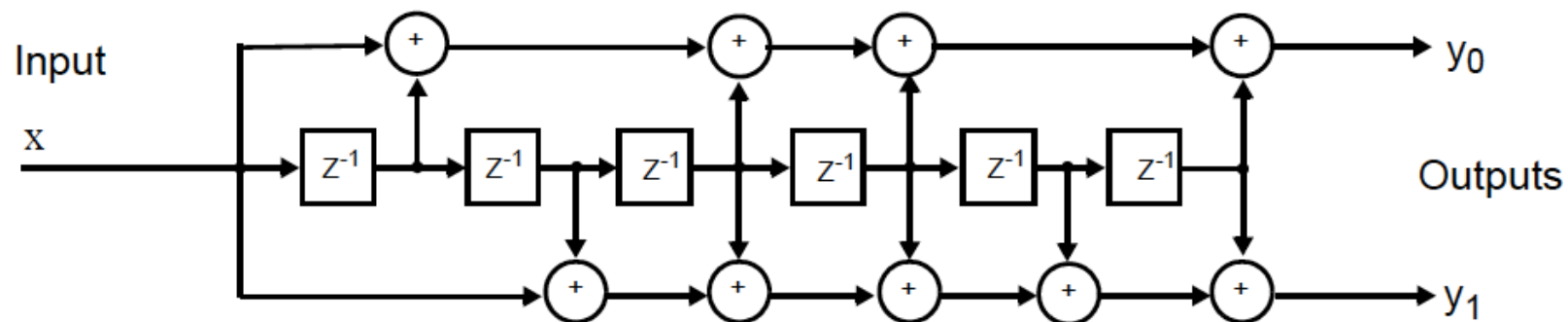
Packet Binary Convolutional Code (PBCC)

- 64-state BCC



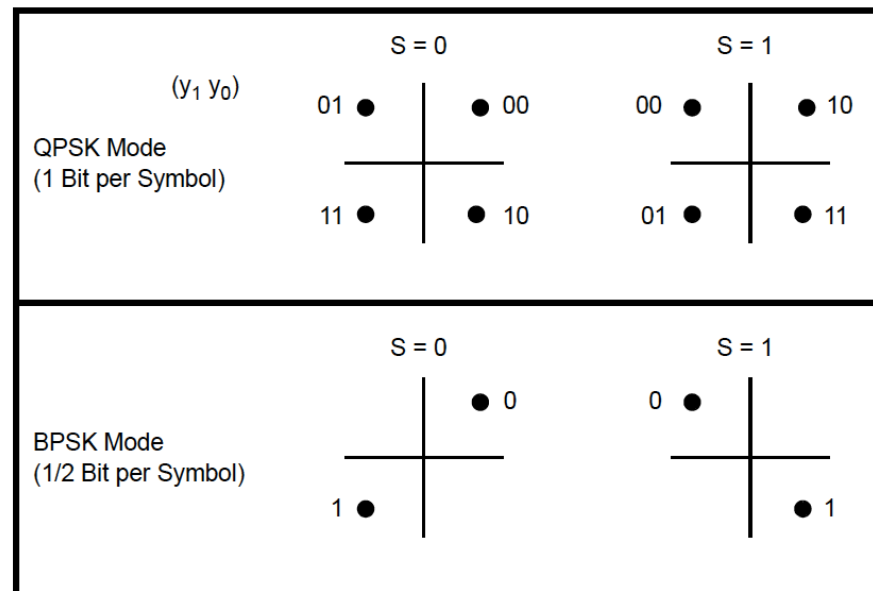
Packet Binary Convolutional Code (PBCC)

- PBCC convolutional encoder
 - Provide encoder the “known state”
 - 6 memory elements are needed and
 - one octet containing all zeros is appended to the end of the PPDU prior to transmission
 - One more octet than CCK
 - For every data bit input, two output bits are generated



Packet Binary Convolutional Code (PBCC)

- For 11Mbps, two output bits (y_0, y_1) produce one symbol via QPSK
 - one data bit per symbol
- For 5.5Mbps, each output bit (y_0 or y_1) produces two symbols via BPSK
 - One-half a bit per symbol



Packet Binary Convolutional Code (PBCC)

- Pseudo-random cover sequence
 - use 16-bit seed sequence (0011001110001011)
 - to generate 256-bit pseudo-random cover sequence

c0 c1 c2 c3 c4 c5 c6 c7 c8 c9 c10 c11 c12 c13 c14 c15
c3 c4 c5 c6 c7 c8 c9 c10 c11 c12 c13 c14 c15 c0 c1 c2
c6 c7 c8 c9 c10 c11 c12 c13 c14 c15 c0 c1 c2 c3 c4 c5
c9 c10 c11 c12 c13 c14 c15 c0 c1 c2 c3 c4 c5 c6 c7 c8
c12 c13 c14 c15 c0 c1 c2 c3 c4 c5 c6 c7 c8 c9 c10 c11
c15 c0 c1 c2 c3 c4 c5 c6 c7 c8 c9 c10 c11 c12 c13 c14
c2 c3 c4 c5 c6 c7 c8 c9 c10 c11 c12 c13 c14 c15 c0 c1
c5 c6 c7 c8 c9 c10 c11 c12 c13 c14 c15 c0 c1 c2 c3 c4
c8 c9 c10 c11 c12 c13 c14 c15 c0 c1 c2 c3 c4 c5 c6 c7
c11 c12 c13 c14 c15 c0 c1 c2 c3 c4 c5 c6 c7 c8 c9 c10
c14 c15 c0 c1 c2 c3 c4 c5 c6 c7 c8 c9 c10 c11 c12 c13
c1 c2 c3 c4 c5 c6 c7 c8 c9 c10 c11 c12 c13 c14 c15 c0
c4 c5 c6 c7 c8 c9 c10 c11 c12 c13 c14 c15 c0 c1 c2 c3
c7 c8 c9 c10 c11 c12 c13 c14 c15 c0 c1 c2 c3 c4 c5 c6
c10 c11 c12 c13 c14 c15 c0 c1 c2 c3 c4 c5 c6 c7 c8 c9
c13 c14 c15 c0 c1 c2 c3 c4 c5 c6 c7 c8 c9 c10 c11 c12